

An Area Efficient Orthogonal Multibeamforming for MIMO System

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Abstract: The implementation of multiple antennas at both ends of the link is widely considered as an attractive solution to substantially improve the overall system performance. The key aspect that allows multi-beam forming systems to improve the wireless communication systems from the additional degrees of freedom provided by the spatial dimension. The use of multiple directional path for each antennas in combination with advanced approximation algorithms, give rise to FFT model, which is able to boost the spectral efficiency and enhance the link reliability. To that end, the radio based communications are resorting to multicarrier modulations and spatial diversity and it is regarded as the dominant technology. On one hand, the FFT is able to accommodate multi-antenna configurations in a very straightforward manner. On the other hand, the approximations exhibited by the based on numerous Techniques, which may substantially reduce the complexity. Simulation results depict the performance of multi beam forming techniques. Hardware synthesis results shows the performance metrics of approximations.

I. Introduction

Spatially propagating signals encounter the presence of interfering signals and noise signals. If the desired signal and the interferers occupy the same temporal frequency band, then temporal filtering cannot be used to separate the signal from the interferers. However the desired and the interfering signals generally originate from different spatial locations. This spatial separation can be exploited to separate the signals from the interference using a beamformer. A beamformer consists of an array of sensors in a particular configuration. The output of each sensor is properly filtered and the filtered outputs of all the sensors are added up.

Typically a beamformer linearly combines the spatially sampled waveform from each sensor in the same way a FIR filter linearly combines temporally sampled data. When low frequency signals are used an array of sensors can synthesize a much larger spatial aperture than that practical with a single physical antenna. A second very significant advantage of using an array of sensors is the spatial filtering versatility offered by discrete sampling. In many applications it is necessary to change the spatial filtering function in real time to maintain effective suppression of interfering signals. Changing the spatial filtering function of a continuous aperture antenna is impractical. Typical uses of beamforming arise in RADAR, SONAR, communications, imaging, Geophysical exploration, Biomedical and also in acoustic source localization.

The goal of cooperative diversity is to increase the reliability and the quality of service (QoS), coverage area range, and the data throughputs as well as improve the spectral efficiency of the wireless networks while prolonging the life of the nodes or user terminals by increasing energy efficiency. In a network consisting of independent users (ad hoc networks), achieving full diversity depends on the successful use of distributed coding and routing algorithms.

1.2 Alamouti Scheme

The Alamouti scheme can be extended to a system with $2n \times 2n$ antenna elements. Initially, it was introduced as a code which could achieve full diversity in a flat fading channel. Later a modified version for multipath fading channels was proposed for the single-antenna receiver case. Then system was expanded to the two-antenna receiver case. This thesis will investigate the performance of the distributed form of decode-and-forward and of Alamouti space time coding, which provide spatial diversity in clustered multihop relay networks.

1.3 MIMO

The Multiple-Input Multiple-Output channel with M_1 transmitting and M_2 receiving antennas are depicted in Fig 1.1. In this section the capacity results and the optimal power allocation strategy are summarized. The derivation of the capacity of the MIMO channel first appeared by Teletar, and since then, MIMO channels have been subject to a massive amount of research.

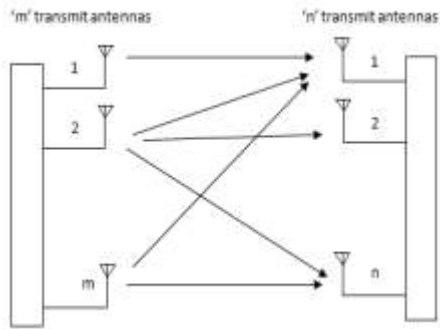


Fig 1.1 MIMO

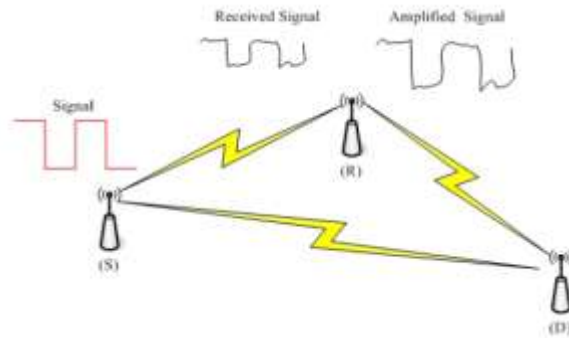


Fig 1.2 Relay based network

MIMO channels, as opposed to Single-Input Single-Output (SISO) channels, not only increases the throughput under the same power constraints, but also makes the channels more robust to fading and enables the possibility of creating multiple separate spatial channels. These properties are termed to transmit diversity and spatial multiplexing, respectively.

1.4 Relay Channel

The shared relay is one of the identified sub networks, is addressed. The system model is depicted in Fig. 1.2 and consists of two base stations B1 and B2, and two terminals T1 and T2, that are paired such that B_i and T_i, with $i \in \{1, 2\}$, wish to attain two-way communication. All nodes are assumed to be half-duplex, there are no direct links between the base stations and the terminals. The relay and the base stations are each equipped with 2M antennas and the terminals have M antennas.

In this network, the rates of each of the communication flows are denoted by R_i and R_{Bi}, i.e. the rate of the communication flow from terminal i to base station and from base station i to terminal i, respectively. The objective is to find the best achievable rates subject to a certain performance metric. In this thesis, the Weighted Minimum Rate (WMR) performance metric is used. The metric is defined as

$$\text{WMR}(R_{B1}, R_1, R_{B2}, R_2) = \min(w_1 R_1, w_{B1} R_{B1}, w_2 R_2, w_{B2})$$

II. Literature Survey

We describe about the problem which is present on the existing problem and the methods to overcome these problems in the future projects. This chapter also describes about the literature review and the feasibility studies involved.

J. Nicholas Laneman, David N. C. Tse and Gregory W. Wornell “Cooperative Diversity in Wireless Networks: Efficient Protocols and Outage Behavior” says that the underlying techniques exploit space diversity available through cooperating terminals' relaying signals for one another. We outline several strategies employed by the cooperating radios, including fixed relaying schemes such as amplify-and-forward and decode-and-forward. We develop performance characterizations in terms of outage events and associated outage probabilities, which measure robustness of the transmissions to fading, focusing on the high signal-to-noise ratio. Thus, using distributed antennas, we can provide the powerful benefits of space diversity without need for physical arrays. Applicable to any wireless setting, including cellular or ad hoc networks-wherever space constraints preclude the use of physical arrays-the performance characterizations reveal that large power or energy savings result from the use of these protocols.

R. Mesleh, and H. Haas and Chang Wook Ahn, and Sangboh Yun “Spatial Modulation - A New Low Complexity Spectral Efficiency Enhancing Technique” says that the multiplexing gain of multiple antenna transmission strongly depends on transmit and receive antenna spacing, transmit antenna synchronization, and the algorithm used to eliminate interchannel interference (ICI) at the receiver. In this paper, a new transmission approach, called spatial modulation, that entirely avoids ICI and requires no synchronization between the transmitting antennas while maintaining high spectral efficiency is presented. A block of information bits is mapped into a constellation point in the signal and the spatial domain, i.e. into the location of a particular antenna. The receiver estimates the transmitted signal and the transmit antenna number and uses the two information to de-map the block of information bits. For this purpose, a novel transmit antenna number detection algorithm called iterative-maximum ratio combining (i-MRC) is presented. Spatial modulation is used to transmit different number of information bits and i-MRC is used to estimate both the transmitted signal and the transmit antenna number. The results are compared to ideal V-BLAST (vertical-Bell Lab layered space-time) and to MRC. Spatial modulation outperforms MRC. The (bit-error-ratio) BER performance and the

achieved spectral efficiency is comparable to V-BLAST. However, spatial modulation results in a vast reduction in receiver complexity.

Rakshith Rajashekar and K. V. S. Hari “Antenna Selection in Spatial Modulation Systems” says that Novel transmits antenna selection techniques are conceived for Spatial Modulation (SM) systems and their symbol error rate (SER) performance is investigated. Specifically, low-complexity Euclidean Distance optimized Antenna Selection (EDAS) and Capacity Optimized Antenna Selection (COAS) are studied. It is observed that the COAS scheme gives a better SER performance than the EDAS scheme. We show that the proposed antenna selection based SM systems are capable of attaining a significant gain in signal-to-noise ratio (SNR) compared to conventional SM systems, and also outperform the conventional MIMO systems employing antenna selection at both low and medium SNRs.

Kyongkuk Cho and Dongweon Yoon “On the General BER Expression of One- and Two-Dimensional Amplitude Modulations” says that Quadrature amplitude modulation (QAM) is an attractive technique to achieve high rate transmission without increasing the bandwidth. A great deal of attention has been devoted to the study of bit error rate (BER) performance of QAM, and approximate expressions for the bit error probability of QAM have been developed in many places in the literature. However, the exact and general BER expression of QAM with an arbitrary constellation size has not been derived yet. We provide an exact and general closed-form expression of the BER for one-dimensional and two-dimensional amplitude modulations, i.e., PAM and QAM, under an additive white Gaussian noise (AWGN) channel when Gray code bit mapping is employed. The provided BER expressions offer a convenient way to evaluate the performance of PAM and QAM systems for various cases of practical interest. Moreover, simple approximations can be found from our expressions, which are the same as the well-known approximations, if only the dominant terms are considered.

III. MIMO Channel

3.1 INTRODUCTION

Multiple input multiple output is a radio communication or RF technology. MIMO technology has been standardized for wireless LANs, 3G mobile phone networks and 4G mobile phone networks. MIMO is sub divided into three main categories, precoding, spatial multiplexing and diversity coding.

Conventional beamforming can be divided into several approaches based on the type of antennas that are used. One approach is fixed multi-beam, involves generating a set of beams by using a set of distinct aperture antennas, such as horn, lens or reflector antennas, to provide one spot beam per cell. Cell size is determined by beampattern of the individual antennas. Aperture antennas can achieve beam patterns with low side lobes levels and improve the system capacity. But the antenna size and weight could be significant, which means that a heavy system payload may be required.

3.2 optimum Complex Multiplier Unit

As shown in Fig. 3.1 it contains 2 multiplexers (M1 and M2), 1.5-word memory (G1, G2, and G3), 2 Real Multipliers and 1 Real Adder. The signal s controls the behavior of two multiplexers (M1 and M2): through or swap. The signal s also controls the behavior of the Real Adder, which supports both addition and subtraction operations. For the input couple $(0-r, 8-r)$ and $(0-i, 8-i)$ at the Node-Cin Table II the sum part data $0-r$ and $0-i$ will directly pass to the delay memory G1 to generate $0-r^*$ and $0-i^*$ with one cycle delay in consecutive two cycles, while the difference part $8-r$ and $8-i$ will directly enter the Real Multipliers (Node-D) to generate $(c \times 8-r, d \times 8-r)$ and $(c \times 8-i, d \times 8-i)$ before reordering. The reordering process is performed as follows.

1) In the first cycle, when $8-r$ comes, the signal s ($s = 1$) selects “through”; that is, the up (down) input of the multiplexer (M1 or M2) connects to the up (down) output. Then, the G2 (or G3) would be $d \times 8-r$ (or $c \times 8-r$) in the second cycle.

2) In the second cycle, when $8-i$ comes, the signal s ($s = 0$) selects “swap”; that is, the up (down) input of the multiplexer (M1 or M2) connects to the down (up) output. Then, the G2 (or G3) would be $c \times 8-i$ (or $d \times 8-r$) in the third cycle. The s will make the Real Adder perform subtraction operation and then $c \times 8-r - d \times 8-i$ ($8-r^*$) would appear at the Node-E.

3) In the third cycle, the signal s ($s = 1$) selects “through” for M1 and M2, and chooses addition operation for Real Adder. Then, $d \times 8-r + c \times 8-i$ ($8-i^*$) would appear at the Node-E.

3.3 Processing Element:

The butterfly units will perform complex additions and subtractions of two complex input data

- $x[n]$
- $x[n+N/2]$ where $N = \text{FFT length}$

In most case delay elements are used for data storage.

- SHIFT REGISTER.
- Dual port RAM.
- FIFO
- Simple BUFFER

Here we use FIFO as a delay element. All input values are saved into the FIFO until the $N/2$ input reached with current input. Then, the butterfly units conduct calculations between the current input values and FIFO outputs. From the butterfly unit outputs, the complex addition outputs will be forwarded into next stage. And, the complex subtraction outputs will be entering into the FIFO.

BU1 will perform complex addition and subtraction.

A. And BU2 will perform twiddle factor $-j$ multiplication with the help of multiplexers and control signals.

B. MUX based bypass circuits are used to control FIFO input and butterfly computation input.

C. FIFO length will be changed based on number of FFT points used and also based on FFT stage.

Here we consider 64 bit complex number with

- 32 bit real part (MSB).
- 32 bit imaginary part (LSB).

Real and imaginary values are computed separately.

IV. Hardware And Software Used

4.1 Simple Asic Design Flow

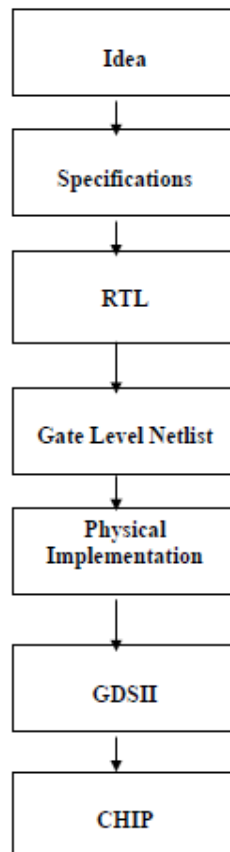


FIG 3.3: SIMPLE ASIC DESIGN FLOW

For any design to work at a specific speed, timing analysis has to be performed. We need to check whether the design is meeting the speed requirement mentioned in the specification. This is done by Static Timing Analysis Tool, for example Primitime.

4.2 Fpga Design Flow

The standard FPGA design flow starts with design entry using schematics or a hardware description language (HDL), such as Verilog HDL or VHDL. In this step, you create the digital circuit that is implemented inside the FPGA. The flow then proceeds through compilation, simulation, programming, and verification in the

FPGA hardware we first define the relevant terminology in the field and then describe the recent evolution of FPDs. The three main categories of FPDs are delineated: Simple PLDs (SPLDs), Complex PLDs (CPLDs) and Field-Programmable Gate Arrays (FPGAs).

V. Circuit Topologies, Beamforming Architectures

Realization of the analog-DFT is key to implementing the mmW receiver and transmitter architectures. Early attempts to implement analog DFT processors used opamp circuits to realize the weights of the DFT matrix.

This approach is slow and difficult to scale to larger arrays because the twiddle factors become closer to each other as the FFT size increases, making them harder to realize accurately. More recently, a 0.13 μm CMOS 8-point Cooley-Tuckey FFT processor for orthogonal frequency division multiplexing (OFDM) applications was reported. The processor uses a time-interleaving bank of sample-and-holds and discrete time analog multipliers, and has been tested with 1 GS/s OFDM inputs. However, dedicated input signals are used to represent the FFT coefficients, which makes scaling difficult. 2-D rectangular LC lattices implemented on CMOS have also been proposed for computing analog DFTs of spatial input signals.

The method has been verified using numerical simulations, and bandwidths of > 10 GHz are possible for onchip implementations. However, such large bandwidths require small inductor and capacitor values, which are difficult to realize accurately, and unwanted mutual coupling between the inductors is also an issue. The analog FFT processor in uses a current-mirror-based architecture to scale the input current by the twiddle factor weights. However, the authors had to approximate the weights to the first decimal place for ease of implementation, resulting in degraded beam shapes. Finally, the work in describes a 16-point analog domain FFT using a charge-reuse analog Fourier transform (CRAFT) engine. The circuit uses charge reuse to achieve an input bandwidth of 5 GHz. However, the design requires RF samplers in the front-end, and inaccuracies in the capacitance network lead to twiddle factor errors that make scaling difficult.

VI. Results

6.1 Beamangle And Distance Metrics

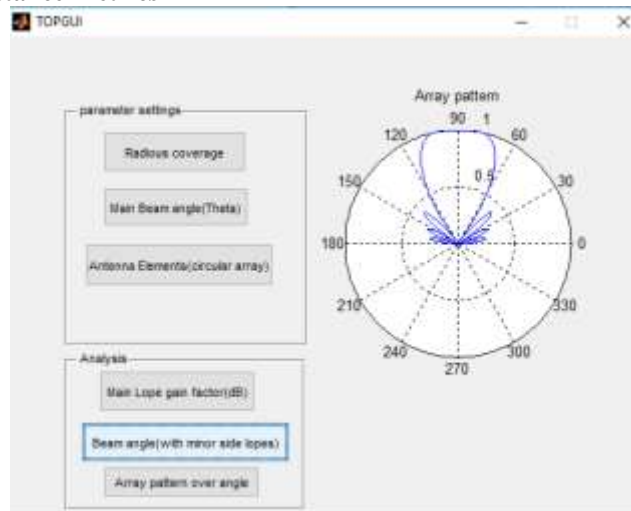


Fig. 6.1 (a) Beam forming analyses over combined beam angle & distance metrics

The above figure describes the result of Beamangle with one main lobe and many side lobes. Due to maximum cover area and antenna element the main lobe becomes stringent and the side lobes are suppressed

6.2 Performance Of Beamforming

Beamforming is a signal processing technique used in sensor arrays for directional signal transmission or reception. By maintaining the coverage radius and the antenna element to be moderate, the side lobes get varied with respect to the beam angle. The below figure shows the performance of beamforming over various beamangle.

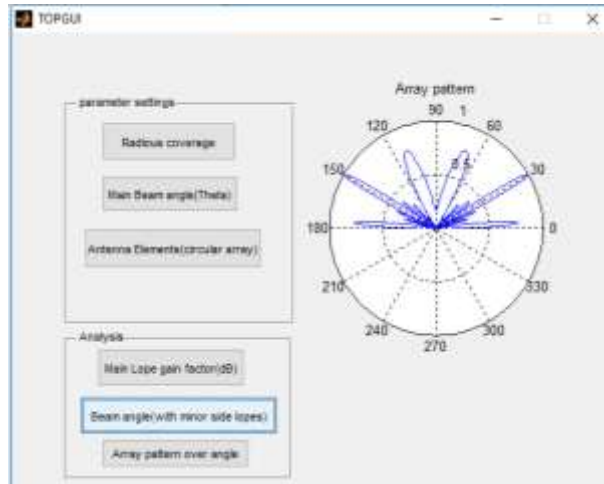


Fig 6.2(a) Performance of beam forming process over various beam angles

6.3 Array Pattern Over Angles

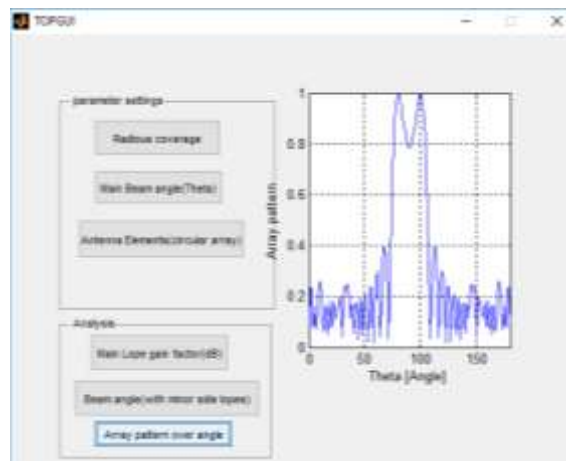
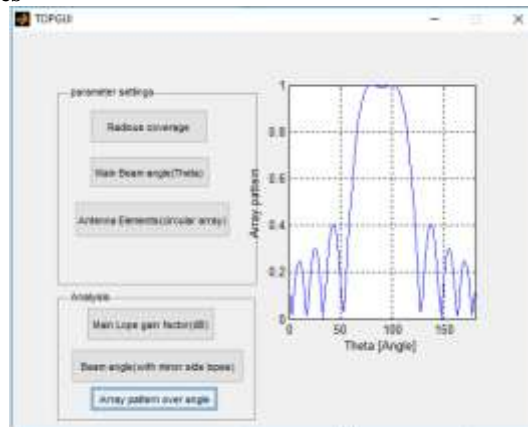


Fig 6.3 Array pattern over angles

6.4 Beam Angle Depending On Antenna Element

The above figure shows that as the number of antenna element increases the side lobes are suppressed .So as per the need of the side lobes the antenna elements can be considered

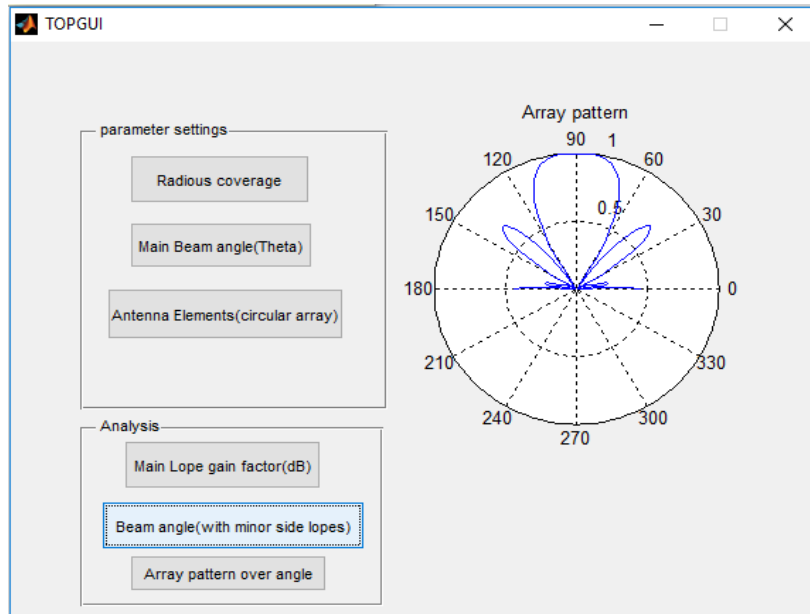


Fig 6.4 Beam angle over element

6.5 Gain Factor

By the lobe gain factor it is evident that, the numbers of side lobe are less for small coverage radius and there are comparatively many side lobes for larger coverage distance. Thus as per the requirement of side lobe in transmission the radius coverage can be altered.

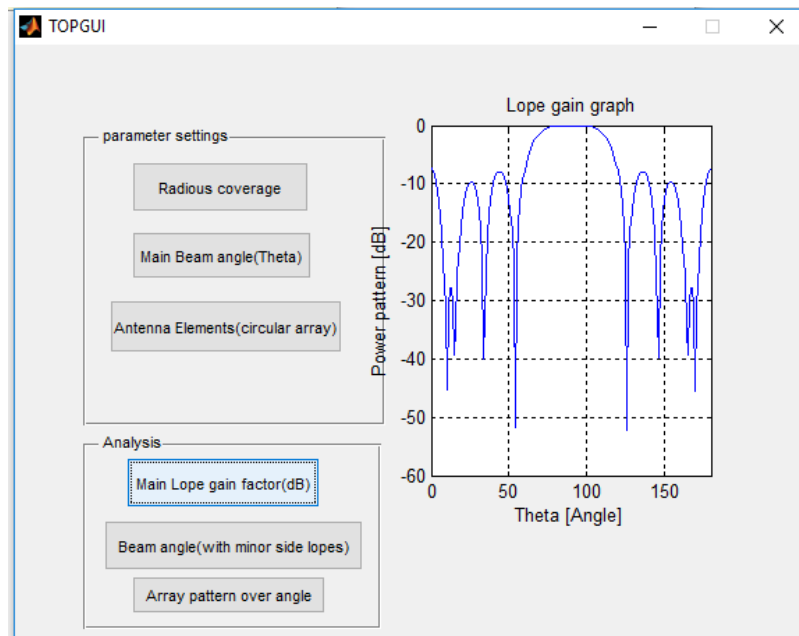


Fig 6.5 Gain Factor

6.2 Area Utilization Report:

Flow Summary	
Flow Status	Successful - Sat Oct 19 02:36:01 2013
Quartus II Version	9.0 Build 132 02/25/2009 SJ Web Edition
Revision Name	fft
Top-level Entity Name	radix_2_4_top
Family	Cyclone III
Met timing requirements	N/A
Total logic elements	1,574 / 39,600 (4 %)
Total combinational functions	1,550 / 39,600 (4 %)
Dedicated logic registers	1,336 / 39,600 (3 %)
Total registers	1336
Total pins	482 / 536 (90 %)
Total virtual pins	0
Total memory bits	0 / 1,161,216 (0 %)
Embedded Multiplier 9-bit elements	0 / 252 (0 %)
Total PLLs	0 / 4 (0 %)
Device	EP3C40F780C6
Timing Models	Final

Figure 6.2 .Flow summary report

6.3 Performance Report:

Pin	Pinched Pin	Clock Name	Note
100.00MHz	200.00MHz	clk	

This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of different clocks, including generated clocks, are ignored. For paths between a clock and its inverter, FMAX is computed as if the rising and falling edges are scaled along with FMAX, such that the duty cycle (in terms of a percentage) is maintained. Altera recommends that you always use clock constraints and other clock reports for sign-off analysis.

Figure 6.3.Fmax. Summary report

6.4 Synthesis Report:

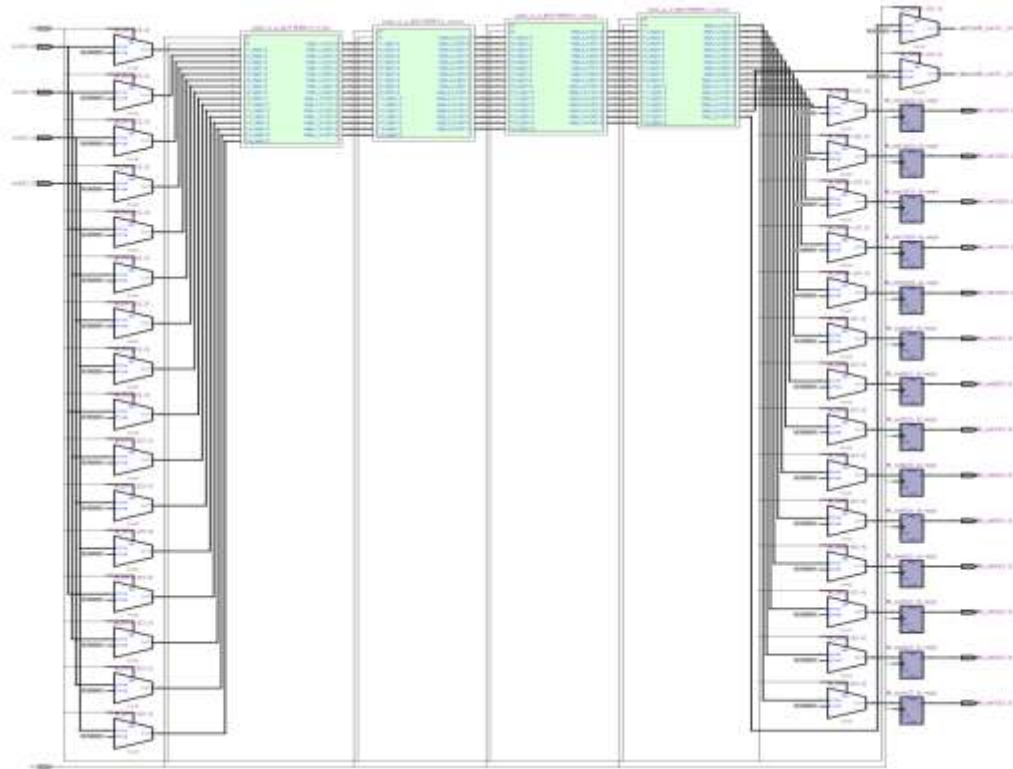


Figure 6.4 RTL Schematic report.

6.5 Map Viewer:

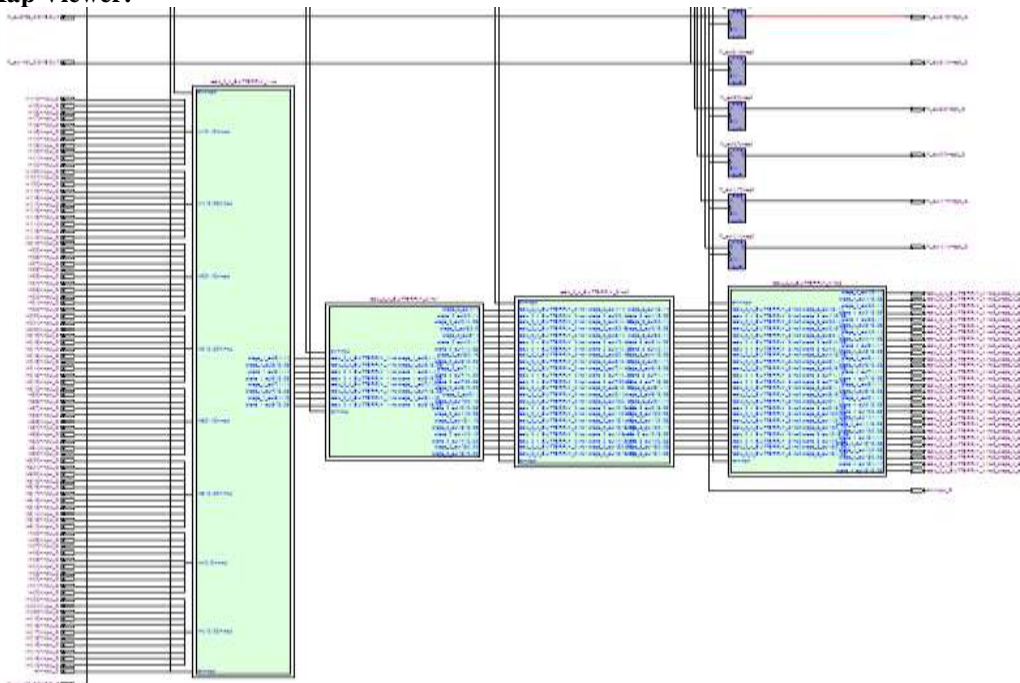


Fig 6.5 Technology map viewer

Reference

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